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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,122	01/02/2002	David G. Scott	FIS9-2001-0396US1	8789

34313 7590 10/08/2003

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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,122	SCOTT ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *3-5,8 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) (3 sheets)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Objections

Claims 3, 4, 5, 8, 10, 11, 12, and 13 are objected to because of the following informalities: as per claims 3, 4, 10, 11, 13, the duplicate lettering of steps is confusing; as per claim 5, "." [line 3, second occurrence] should be deleted; as per claim 8, "set" and "point" [line 1] should both be plural; as per claim 10, ":" [line 2, either occurrence] should be deleted; as per claim 12, the claim cannot be dependent upon itself and "." [line 3, second occurrence] should be deleted; as per claim 13, "d)" [line 1] should be changed to --e)--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 4, the antecedent basis for "step b)" [line 1] is confusing since claims 1 and 3 both have a step "b)". Also, the "wherein" clause is confusing, perhaps the term --applying-- was omitted?

As per claim 5, the antecedent basis for "step c)" [line 1] is confusing since claims 1, 3, and 4 all have a step "c)".

As per claim 6, step "g)" is confusing because it is not clear what "the measure of testability for the IC" is being compared to.

As per claim 9, there is no antecedent basis for the features recited in this claim.

As per claims 14 and 15, there is no antecedent basis for "the population" [lines 2, 5, 1, respectively]. Further as per claim 15, the antecedent basis for "when comparing the respective testability of the individual sets" [lines 2-3] is not clear.

The remaining claims, though not specifically mentioned, are rejected for incorporating the errors of their respective base claims by dependency.

The following rejections are based on the examiner's best interpretation of the claims in view of the issues raised above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by O'Dare et al. ["System design for test using a genetically based hierarchical ATPG system"].

As per claims 1 and 17, O'Dare et al. disclose a method and program storage device [page 9/1, Introduction], said method comprising: a) determining a measure of testability for the IC [pages 9/2-9/3, section 2.1]; b) selecting test point candidates to be evaluated for insertion in said IC and arranging said test point candidates into a first plurality of pairs of sets [pages 9/1-9/2, section 1.1]; c) evaluating said first plurality of pairs of sets and forming a second plurality of pairs of sets, said evaluation being based on the respective testability improvement achieved by each plurality of said pairs of sets, and recombining said first and second plurality of pairs of sets based on results from said evaluation [pages 9/1-9/2, section 1.1]; d) repeating step c) until said first and second pairs of sets converge to form a best set, said best set providing the test points to be inserted into the IC [pages 9/1-9/2, section 1.1]; and e) repeating steps a) through d) until all the test points to be inserted have been incorporated into the IC [page 9/3, section 3.1]. As per claim 2, O'Dare et al. further disclose wherein in step a) the measure of testability for the IC is determined by a combination of fault simulation and probability of detection calculations [page 9/2, paragraphs 1-2].

Claims 1-5 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen ["Genetic Algorithm Based Test Generation for Sequential Circuits"].

As per claims 1 and 17, Shen discloses a method and program storage device [section 5], said method comprising: a) determining a measure of testability for the IC

[section 4]; b) selecting test point candidates to be evaluated for insertion in said IC and arranging said test point candidates into a first plurality of pairs of sets [section 2.2]; c) evaluating said first plurality of pairs of sets and forming a second plurality of pairs of sets, said evaluation being based on the respective testability improvement achieved by each plurality of said pairs of sets, and recombining said first and second plurality of pairs of sets based on results from said evaluation [section 2.2]; d) repeating step c) until said first and second pairs of sets converge to form a best set, said best set providing the test points to be inserted into the IC [section 2.2]; and e) repeating steps a) through d) until all the test points to be inserted have been incorporated into the IC [section 2.2]. As per claim 2, Shen further discloses wherein in step a) the measure of testability for the IC is determined by a combination of fault simulation and probability of detection calculations [section 2.2]. As per claim 3, Shen further discloses further including the steps of: performing a fault simulation using a set of random patterns to identify faults detected by the random patterns [sections 4, 5.3, 5.4]; computing a measure of controllability based on the number of times the IC takes a predetermined logic value during fault simulation [section 4]; deriving a measure of observability from the measure of controllability [section 4]; assigning a detection probability of 1.0 to a fault that was detected by the random patterns [section 2.2]; assigning a detection probability for the remaining faults according to the measure of controllability and observability respectively derived from steps above [section 2.2]; and accumulating the detection probability for all faults in the IC [sections 2.2, 5.5]. As per claim 4, Shen further discloses further comprising applying a first selection criteria, comprising:

estimating the testability improvement of the IC derived from inserting the test point based on changes in the measure of controllability and observability [section 4]; measuring the number of faults having a probability of detection nearing 1.0 if an observable point is placed at a particular location in the IC [section 2.2]; and determining cluster roots representing nodes having poor output controllability and good input controllability and using inputs of the cluster roots as candidate test points to be inserted in the IC [section 3; figure 2; section 4]. As per claim 5, Shen further discloses wherein the number of candidate test points is computer as a linear function of the number of gates in the IC until a maximum number of candidate test points is reached [figure 1].

Claims 6-9 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Harmanani et al. ["A genetic algorithm for testable data path synthesis"].

As per claim 6, Harmanani et al. disclose a method comprising: a) determining a measure of testability for the IC [section 1.2]; b) forming a plurality of first sets of test points and determining the size and the number of said plurality of first sets [sections 2, 4.2]; c) evaluating the improvement in the testability of the IC in the presence of said plurality of first sets of test points [section 4.3]; d) performing an inversion and a mutation of said plurality of first sets of test points [section 4.5]; e) intermingling pairs of said first plurality of sets to form a second plurality of pairs of sets with said intermingled pairs of said first plurality of sets [section 4.5]; f) evaluating said first plurality of pairs of sets and said second plurality of pairs of sets to select which first and second pairs of sets should be kept, said selected pairs of sets of said first and second plurality

replacing the original first plurality of pairs of sets [sections 4.5, 4.6]; and g) comparing the measure of testability for the IC to determine whether the selected plurality of first and second pairs of sets converges towards an optimal set to be inserted in the IC as additional test points [section 4.5, 4.6, 5]. As per claim 7, Harmanani et al. further disclose wherein in step b) the size of the sets of test points is determined as a linear function of the number of gates forming the IC and the number of sets of test points thus far inserted, wherein the size of the sets of test points is limited by an arbitrary upper limit, said limit being increased as more sets of test points are inserted into the IC, and wherein the number of sets is determined by dividing the number of test points by the size of the set [sections 1.2, 2, 3]. As per claim 8, Harmanani et al. further disclose wherein in step c) said sets of test points are grouped into a plurality of first sets according to a predetermined selection criteria [section 4.3]. As per claim 9, Harmanani et al. further disclose changes are updated in order to minimize the computational impact of inserting concurrently multiple test points into the IC [section 5]. As per claim 12, Harmanani et al. further disclose refreshing said first plurality of sets of test points to its original state and repeating steps to generate a total number of pairs of test point sets to be intermingled [sections 4.2, 4.5; figure 4]. As per claim 13, Harmanani et al. further disclose said intermingling comprises: selecting at random a crossover starting point and ending point for each pair of sets (X and Y) to be intermingled [section 4.2]; creating a first new set consisting of all the test points in (X) that reside within the starting and the ending points and of all test points in (Y) that are outside the starting and ending point [section 4.4]; and creating a second new set consisting of all the test

points in (X) that reside outside the crossover starting and ending points and consisting of all test points in (Y) that are inside the crossover starting and ending points, said first and second new sets forming a pair of new sets [section 4.5]. As per claim 14, Harmanani et al. further disclose determining if the pair of new sets should be kept by determining if the testability of either set of the new pair of sets is better than the best testability achieved by either set of the original pair of sets, and else removing the new pair of sets from the set of the original pair of sets [sections 4.3, 4.4, 4.5, 4.6, 5]. As per claim 15, Harmanani et al. further disclose determining whether the sets of test points has converged and whether convergence criteria have been met [section 5].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harmanani et al.

As per claim 11, Harmanani et al. disclose the features from which the claim depends, however, Harmanani et al. do not teach pairing said sets of test points by selecting at random first and second sets of test points, selecting the first and second member of said pair according to which set has the higher testability, forming iteratively subsequent pairs and repeating. A person of ordinary skill in the art at the time of the invention would have found it obvious to pair said sets of test points in Harmanani et al.

because this would improve the computing capabilities of the algorithm by enabling a smaller design space to be operated upon. As per claim 16, a person of ordinary skill in the art at the time of the invention would have found it obvious to process the Harmanani et al. algorithm with parallel processing because of the savings in time gained by such resources.

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: although Harmanani et al. describe performing an inversion and a mutation as cited above, the prior art of record merely discloses that an inversion operator was experimented with, which does not seem sufficient to anticipate or obviate the specifically claimed language.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The applicant is encouraged to review the references cited on PTO-892 as each provides highlighted subject matter that the examiner found to be particularly related to the claim language presented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER